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FIG. 1
(PRIOR ART)

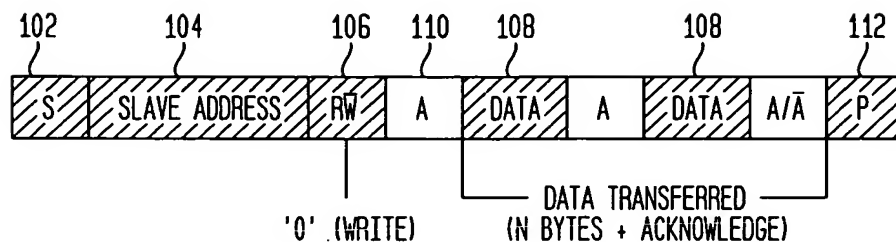| 102	104	106	110	108		108		112
S	SLAVE ADDRESS	R$\overline{W}$	A	DATA	A	DATA	A/$\overline{A}$	P

'0' (WRITE)

DATA TRANSFERRED
(N BYTES + ACKNOWLEDGE)

▨ FROM MASTER TO SLAVE

☐ FROM SLAVE TO MASTER

A = ACKNOWLEDGE (SDATA LOW)
$\overline{A}$ = NOT ACKNOWLEDGE (SDATA HIGH)
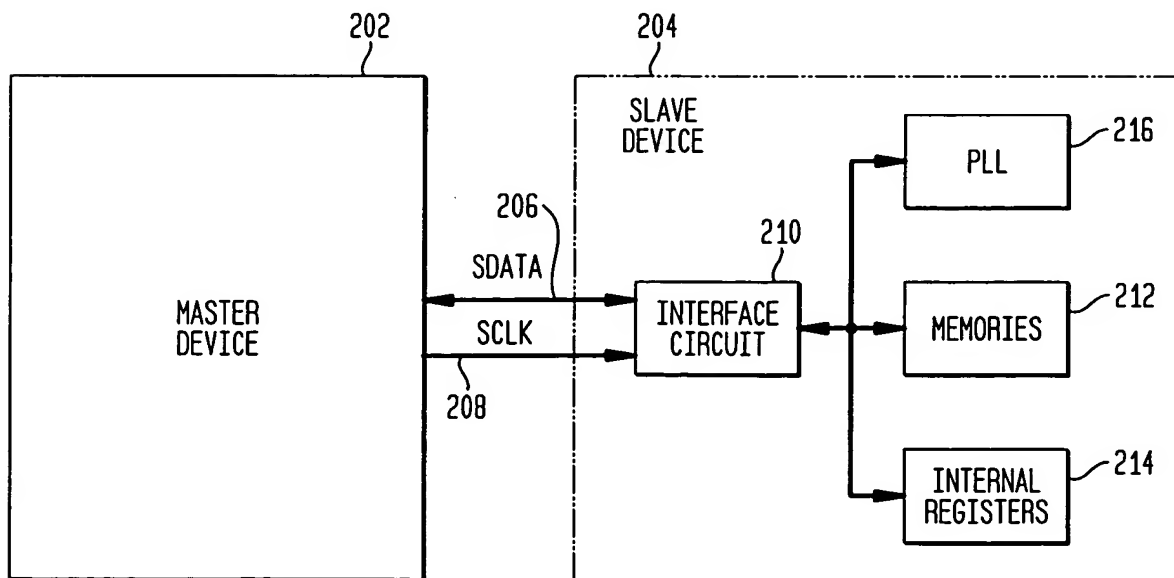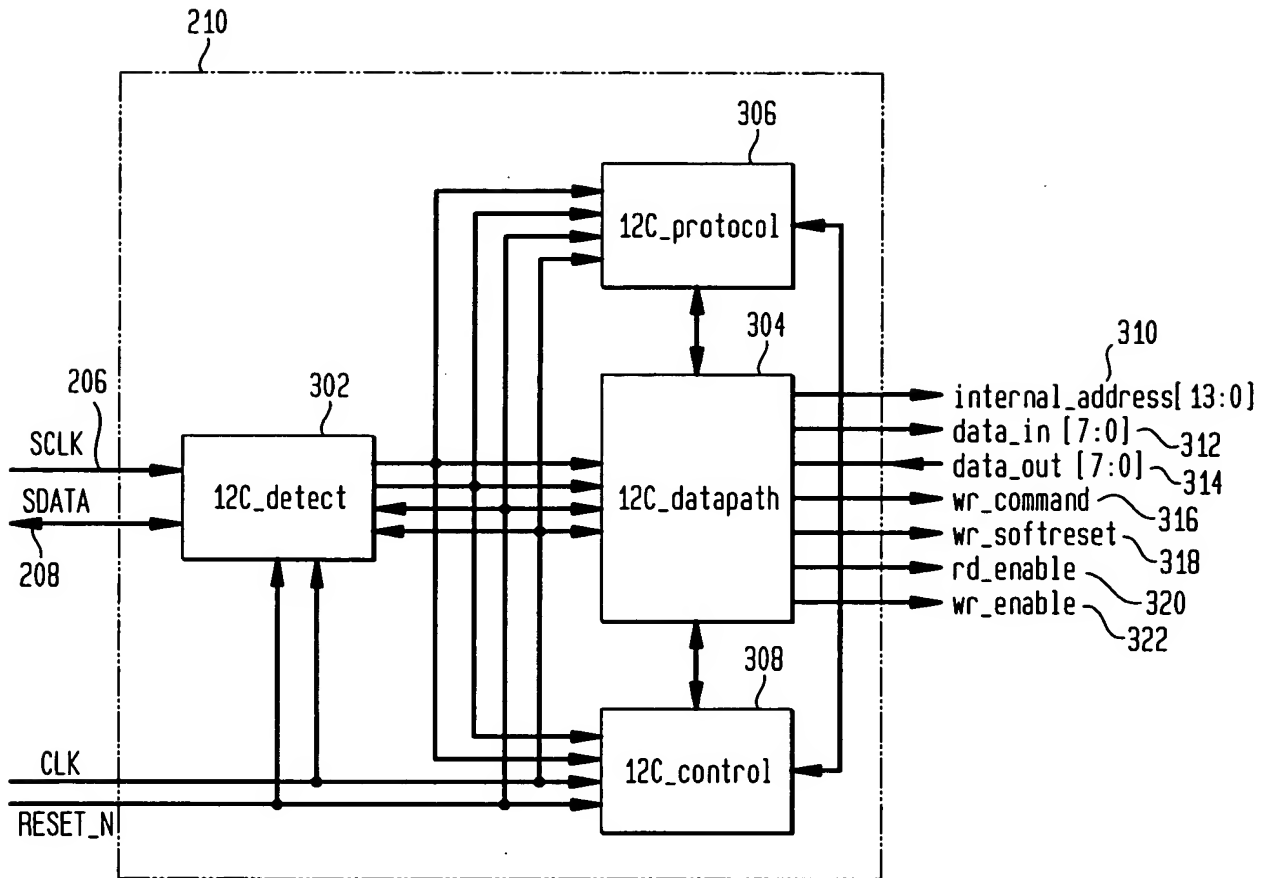S = START CONDITION
P = STOP CONDITION

FIG. 2

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FIG. 3

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FIG. 4

102	104	106	110		110	404	108		108		108		108		108	112
START	SLAVE ADDRESS 1st 7 BITS	R/W 0	ACK 0	COMMAND CODE 01xxxxxx	ACK 0	internal_address[7:0] 8 BITS	ACK 0	Data1 8 BITS	ACK 0	Data2 8 BITS	ACK 0	DataN 8 BITS	ACK 0	STOP

(402)

WHERE XXXXXX ARE internal_address[13:8]

FIG. 5

102	104	106	110	402	110	108	110	108	110	108	110	108	110	108	110	112
START	SLAVE ADDRESS 1st 7 BITS	R/W 0	ACK 0	COMMAND CODE 00xxxxxx	ACK 0	Data1 8 BITS	ACK 0	Data2 8 BITS	ACK 0	Data3 8 BITS	ACK 0	DataN 8 BITS	ACK 0	STOP

WHERE XXXXXX ARE internal_address[5:0]
AND internal_address[13:8] ARE SET TO ZERO'S

FIG. 6

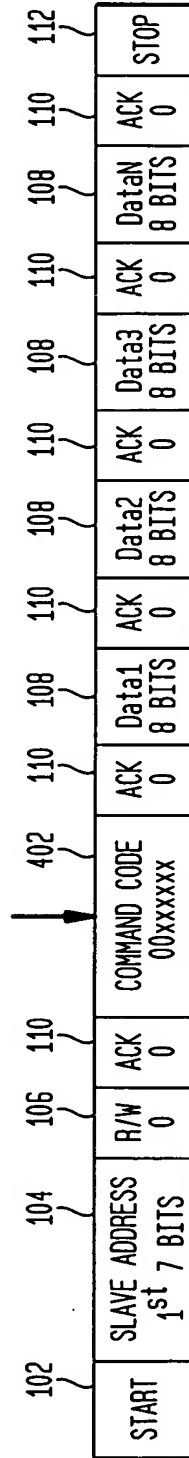| 102	104	106	110	402	110	112
START	SLAVE ADDRESS 1st 7 BITS	R/W 0	ACK 0	COMMAND CODE 11xxxxxx	ACK 0	STOP

WHERE XXXXXX IS THE DESIRED WRITE COMMAND TO SELECTED REGISTERS